QUATERNARY PULSE POSITION MODULATION ELECTRONICS FOR FREE-SPACE LASER COMMUNICATIONS

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Abstract

The development of a high-data-rate communications electronics subsystem for future application in free-space, direct-detection laser communications is described. The dual-channel subsystem uses quaternary pulse position modulation (QPPM)* and operates at a throughput of 650 megabits per second. Transmitting functions described include source data multiplexing, channel data demultiplexing, and QPPM symbol encoding. Receiving functions include analog signal conditioning, slot and symbol clock recovery, QPPM data recovery and decoding, channel data multiplexing, and destination data demultiplexing. Implementation of a prototype version in discrete gallium arsenide logic, radiofrequency components, and microstrip circuitry is presented. The approach to developing an integrated package for potential spaceflight demonstration is described. Link effects simulation, full-duplex data and video communications demonstration, and computer control and monitoring approaches are discussed. Packaging of the communications electronics subsystem and plans for future development conclude the paper.

Introduction

In support of a flight system development and demonstration (FSDD) of a free-space optical communications system

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*Acronyms are defined in a glossary at the end of this paper.

using laser transmitters and direct-detection receivers, NASA Lewis Research Center (Lewis) is developing a 650-Mbps quaternary pulse position modulation (QPPM) electronics subsystem. NASA Goddard Space Flight Center (Goddard) sponsors the FSDD and provides the laser transmitters, the telescope, the optical detectors, and the pointing and tracking control subsystems. When completed, the communications electronics subsystem will be integrated into the FSDD testbed and used by Goddard to evaluate the suitability of direct-detection laser communications for near-term use on inter-satellite links.[1]

Under the High-speed Laser Integrated Terminal Electronics (Hi-LITE) Project Lewis is developing the necessary communications electronics, optical link effects simulation, and test and control equipment to demonstrate full duplex, end-to-end data and video communications before integration with the laser transmitters and receivers of the FSDD testbed.

Phased Approach

Two versions of the electronics subsystem are under development for use in separate laser terminals. The "cooperating" terminal electronics (CTE) is designed first for implementation in laboratory prototype hardware to prove the central concepts and to demonstrate compliance with technical specifications. Source data multiplexing and QPPM encoding on the transmitting side, along with clock and data recovery and destination data demultiplexing on the receiving side are all accomplished in discrete gallium arsenide (GaAs) logic. Analog

signal conditioning, automatic gain control, and matched filtering of the received signal are implemented with a combination of discrete components, radiofrequency modules, and microstrip circuitry. Several of the analog designs are based on work conducted under a Goddard grant to Johns Hopkins University.[2]

Drawing heavily on the CTE designs, the "flight-like" terminal electronics (FTE) will demonstrate reduced size and mass and lower power consumption in flight-qualifiable hardware. An application-specific integrated circuit (ASIC) fabricated in a space-qualified process will be developed for the digital functions; advanced surface-mount and hybrid technologies will be used for the analog circuitry.

The electronics subsystems for the two terminals will be nearly identical in functional capability. Both will support communications through two optical links simultaneously, each conveying 325 megabits per second (Mbps) of information. However, the FTE will contain some additional features, such as internal bit-error-detection capability, not found in the prototype.

Subsystem Overview

Figure 1 shows the interconnection of the major functional elements of the Hi-LITE subsystem in a top-level block diagram. The ground support equipment (GSE) provides the digital data and video sources and sinks, the commercial test equipment for performance measurement, and the electronics and ground support controller (EGSC), and a computer for controlling the subsystem hardware and the experiment. The transmitting and receiving portions of both the CTE and the FTE operate independently of each other to offer flexibility in testing. The final major element is the special test equipment (STE) used to simulate optical link signal degradations. Once the communications electronics subsystem is fully functional, the STE is replaced by an optical link.
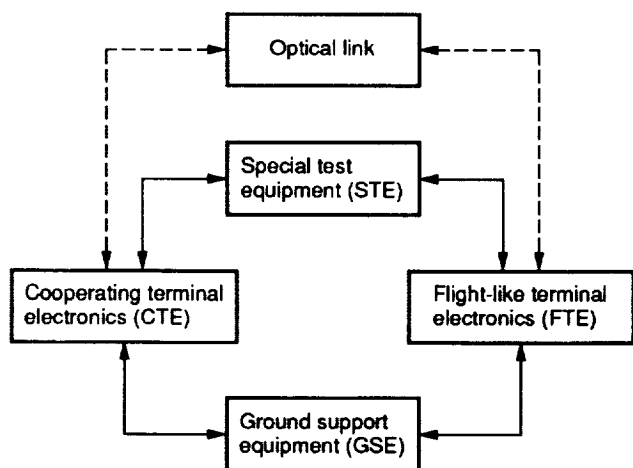

Figure 1.—Top-level block diagram of Hi-LITE subsystem.

Structure of Paper

The next section of this paper provides background on the QPPM format and presents the salient technical specifications for the Hi-LITE subsystem. Details of the transmitting and receiving electronics for the prototype version, the CTE, and the development approach for FTE are described in later sections. Then the digital and analog special test equipment used to simulate optical link effects and the integration and test plans are discussed. Next the GSE, including digital and video data sources, and the computer control and monitoring approach are described. Finally packaging of the communications electronics subsystem and plans for future development conclude the paper.

Background

Quaternary Pulse Position Modulation

M-ary pulse position modulation (PPM) enables multiple bits of information to be transmitted with a single pulse. The modulator encodes k binary information bits into one of $M=2^k$ symbols. The pulse can occupy one of M timeslots in the symbol. Each information bit has a duration of T_b seconds. Because each M-ary PPM symbol represents $k=\log_2 M$ bits, the symbol duration is $T_s=kT_b$ seconds. Therefore the duration of each timeslot in which a pulse can appear is T_s/M seconds.

In optical communications systems the symbol is represented by a single rectangular pulse of the laser in one of the M timeslots in each symbol. The optical pulse duration is never greater than 50% of the bit duration. As M increases beyond 4, the pulse duration becomes a smaller fraction of the bit duration and both the laser pulse duty cycle and the average laser power transmitted decrease. Goddard has specified 4-ary or quaternary PPM for the communications electronics subsystem on the basis of considerations of average and peak-to-average power limitations of the semiconductor lasers under development.

In the Hi-LITE subsystem each group of two information bits is encoded into one of the four QPPM symbols as shown in Fig. 2. A maximum of 650 Mbps of source data is demultiplexed onto two channels, 325 Mbps on each channel. The timing for binary information bits and QPPM symbols along with their synchronized clocks is shown in Fig. 3.

Technical Specifications

The salient technical specifications for the communications electronics subsystem shown in Table I are derived from the FSDD system performance specifications developed by Goddard.[3] These specifications were used to establish design criteria for development of the Hi-LITE demonstration hardware and test equipment.
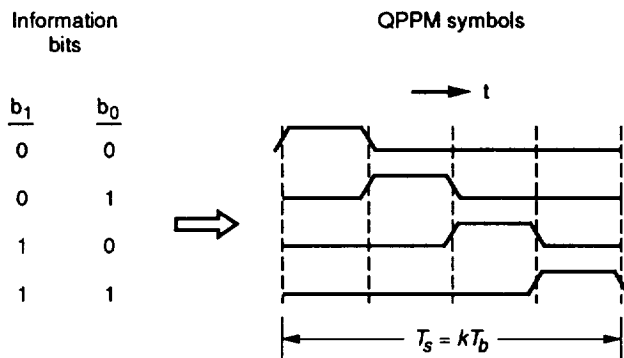
Information bits | QPPM symbols

| b₁ | b₀ |

$$\frac{b_1 \quad b_0}{}$$

b_1	b_0
0	0
0	1
1	0
1	1

$T_s = kT_b$

Figure 2.—Encoding of information bits into QPPM symbols.

$T_b = 6.15$ ns

(a) Binary data (325 Mbps).

3.08 ns

(b) Bit clock (325 MHz).

$T_s = 12.31$ ns

(c) QPPM symbols (325 Msps).

1.54 ns

(d) Slot clock (650 MHz).

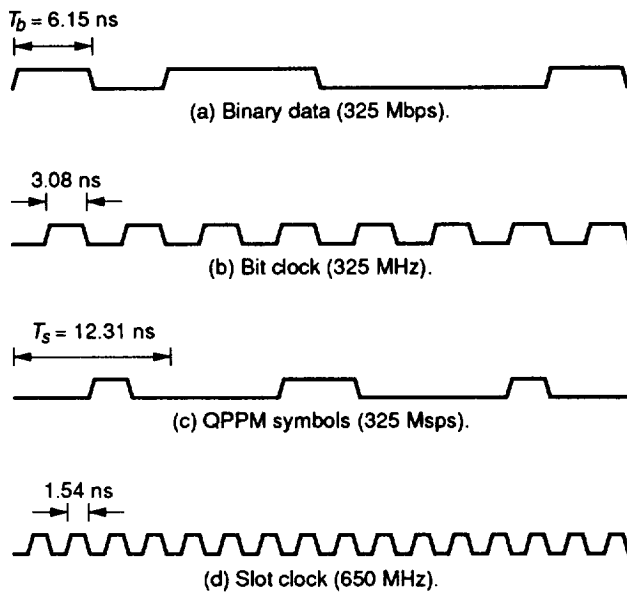Figure 3.—Timing relationship of information data bits and QPPM symbols.

TABLE I.—COMMUNICATIONS ELECTRONICS PERFORMANCE SPECIFICATIONS

Parameter	Specification
Test data sources	Pseudorandom data and digitized video
PRBS pattern length	$2^{23} - 1$ bits
PRBS data rates	325 Mbps, 650 Mbps
Digitized video data rate	325 Mbps
Modulation format	QPPM
Dynamic range	35 dB
Amplitude fluctuation rate	At least 1 kHz
20% to 80% rise and falls times	Less than 200 ps
Experiment control and monitor	Via IEEE–488 or RS–232
Bit-error-rate (BER) measurement interval	As short as 1 ms
Data rate stability	$\pm 2 \times 10^{-6}$
Recovered signal rms tracking jitter	Less than 3% at 10-dB signal-to-noise ratio (SNR)
BER at 10-dB SNR	Less than 1.4×10^{-2}
BER at 17-dB SNR	Less than 1.9×10^{-4}

Hi-LITE Functional Overview

Figure 4 shows the functional elements of the Hi-LITE subsystem described in greater detail later in this paper. Under computer control, data flow from the pseudorandom bit sequence (PRBS) generators and the digitized video sources in the GSE (at the bottom of the figure) up through both channels of the transmitting side of the CTE/FTE (on the left). The transmitting functions include multiplexing source user data as needed, demultiplexing the data into the two channels, and encoding the data into QPPM symbols for eventual transmission by the lasers. The QPPM-encoded data are then either transmitted across the actual optical link or passed as an electrical signal through a link simulation in the STE. The STE uses analog and digital techniques to simulate the fluctuations in signal and noise power, symbol timing jitter, and timing skew between the two channels induced by the optical components and the pointing and tracking subsystem.

The degraded signal is then passed on to the receiving side of the FTE (on the right in Fig. 4). Receiving functions include conditioning the raw electrical signals recovered by the optical receiver, recovering slot and symbol clocks, decoding binary data from recovered QPPM symbols, multiplexing the two channel data streams together, and demultiplexing if necessary for the appropriate destination user.

Finally the digital data are passed to BER measurement equipment or video monitors, tape recorders, and hard-copy units in the GSE for quantitative and subjective analysis. The GSE also contains the computer that selects the different operational modes, controls the test sequences, and collects the performance data.

Cooperating Terminal Electronics

The CTE is divided into the transmitting and the receiving terminal electronics. The transmitting electronics takes the binary digital data from the data sources of the GSE and processes them for transmission by Goddard's cooperating laser terminal. The receiving electronics takes the electrical signals representing the photons detected by the avalanche photodiodes (APD) of the optical receiver and reconstructs as closely as possible the transmitted binary data streams for distribution to the destination sinks in the GSE.

The CTE developed by Lewis under the Hi-LITE project includes several enhancements to earlier communications electronics subsystems developed by Sun and Davidson.[2] The data rate has been increased from 221 to 325 Mbps per optical channel. This data rate enables high-resolution digitized video transmission. A parallel channel at a second optical wavelength has also been added to double the data capacity to 650 Mbps. The second channel creates greater flexibility in system operation by allowing transmission of either two 325-Mbps data streams or a single 650-Mbps data stream. An added feature available in this two-channel version of the CTE
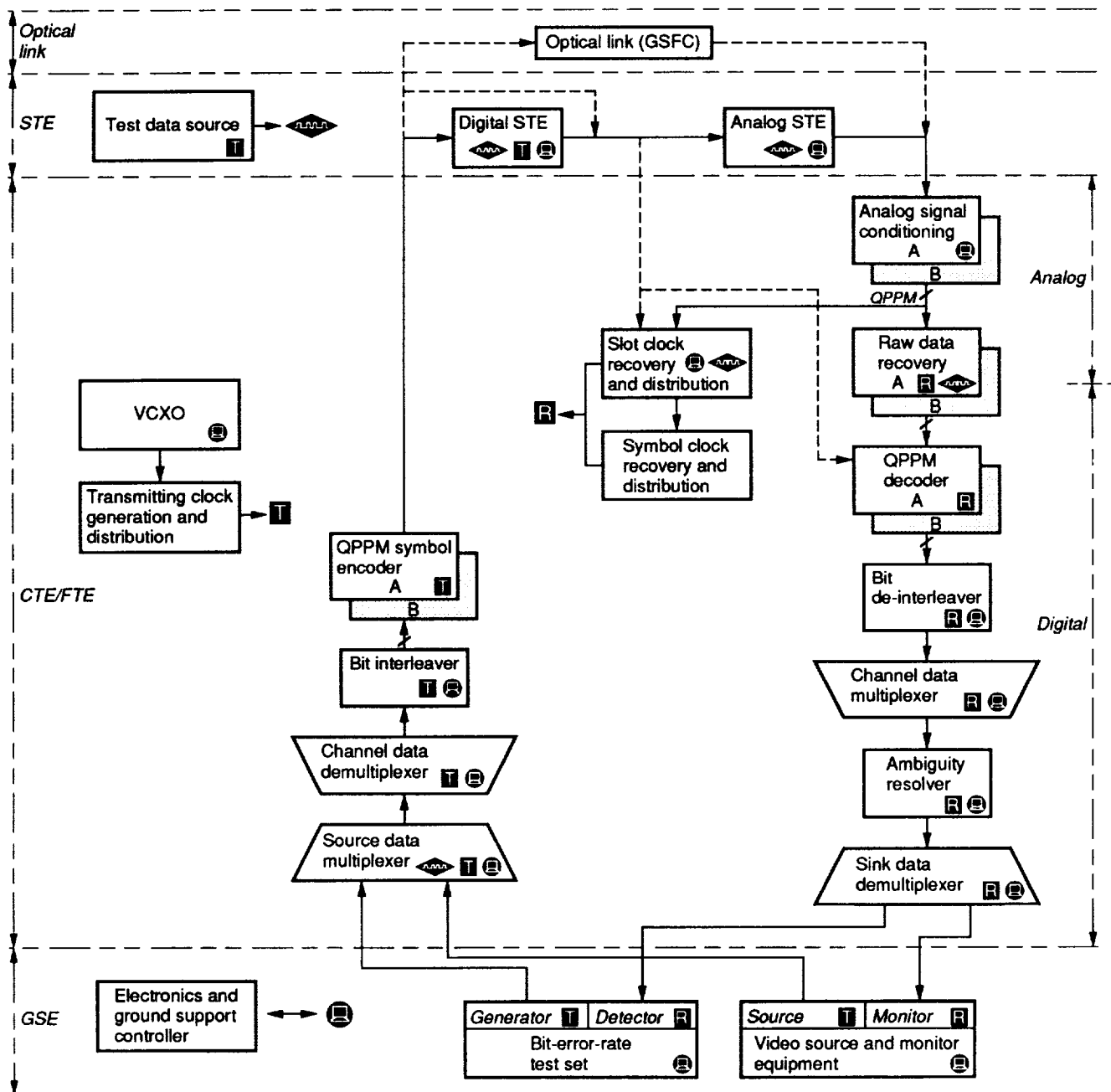
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Figure 4.—Functional block diagram of Hi-LITE subsystems.

is bit interleaving, a method described later that enables BER measurement of non-PRBS data, such as digitized video.

Transmitting Electronics

The transmitting electronics includes four major functions: source data multiplexing; channel data demultiplexing; bit interleaving; and QPPM symbol encoding, as shown in Fig. 5. An ancillary function, clock generation and distribution, is also contained within the transmitting electronics chassis. All digital electronics are implemented in GaAs integrated circuits (IC's) mounted on commercial prototype boards and interconnected with semi-rigid microcoaxial cable.[4]

Source data multiplexer.—The source data multiplexer interfaces the cooperating laser terminal to various data sources. It accepts either a single 650-Mbps signal or two 325-Mbps signals with their accompanying clocks. A control signal from the EGSC selects the source input mode. The input data are latched in flip-flops (F/F) and multiplexed together or passed directly to output flip-flops (depending on the input mode selected), resulting in two 325-Mbps serial data streams. The data sources and the transmitting electronics are all driven by clocks derived from a clock generation and distribution board in the CTE (described later). This is necessary to maintain synchronism within 150 ps between data streams on the two channels.
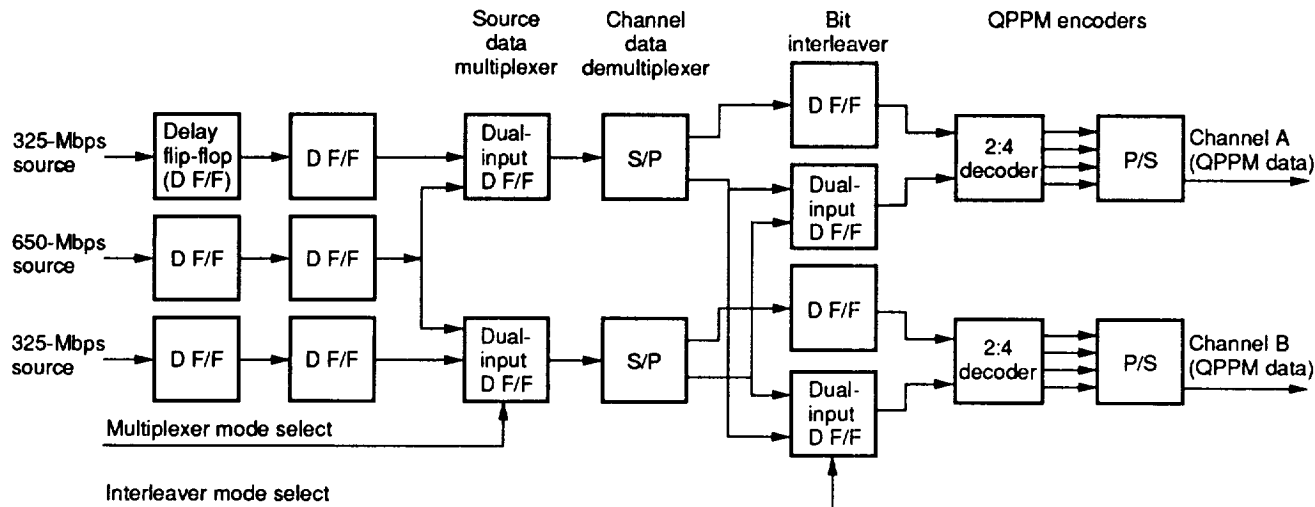
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Figure 5.—Block diagram of CTE transmitting electronics.

Channel data demultiplexer and bit interleaver.—The channel data demultiplexer accepts the two serial 325-Mbps signals from the source data multiplexer and converts them into two 2-bit parallel signals per channel, for a total of four 162.5-Mbps binary data streams. This operation is required because two sequential bits define each transmitted QPPM symbol. Another control signal from the EGSC selects one of two operating modes: direct routing or bit interleaving. In direct routing, two 325-Mbps data streams and clock signals are routed directly to the QPPM symbol encoders. When the bit interleaving mode is selected, data from two 325-Mbps sources are alternately channeled, bit by bit, to the two optical channels. The least significant bits of each 2-bit pair from both sources are exchanged before being encoded into their respective QPPM symbols. This enables the BER performance of the half of an optical link carrying real-time video data to be inferred from the BER measurement of the half carrying the PRBS data. A commercial test set computes the BER on the recovered PRBS data in order to supplant the need for reconstructing and resynchronizing an error-free video data stream for bit-by-bit comparison. Because one-half of each source data set is transmitted on each channel, both sets of source data will experience the same link perturbations and therefore the same BER. This method also allows the performance of the two optical links to be compared by using real data.

Figure 6 shows the two modes. Note how the data from the two sources are split equally into the two channels A and B in the interleaving mode. At this point in the transmitting electronics the rate of each data stream is 162.5 Mbps.

QPPM symbol encoder.—Each QPPM symbol encoder accepts the two 162.5-Mbps parallel data streams for one channel and converts them into a 325-Mbps QPPM encoded data stream. Data streams from both encoders are used to modulate the two lasers.

Clock generation and distribution board.—Each of the boards on the transmitting side of the CTE, along with the

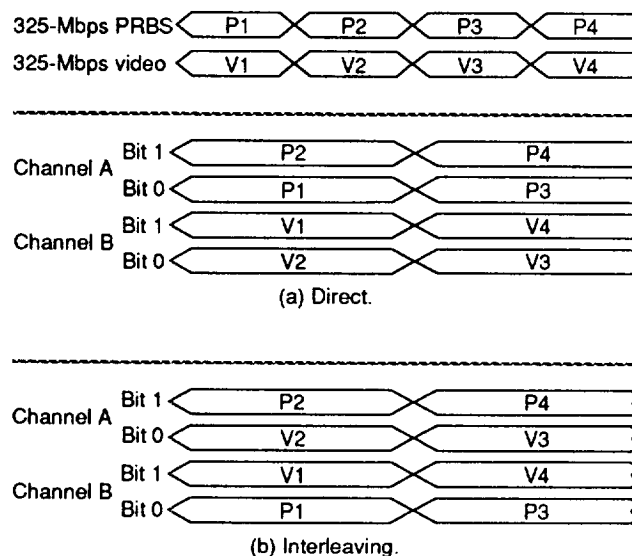(a) Direct.

(b) Interleaving.

Figure 6.—Timing diagram for CTE channel data demultiplexer.

video and data test sources and the special test equipment, require precisely aligned clock signals at the bit clock rate or a submultiple of it to ensure synchronous operation at the laser transmitters. These clock inputs are represented in Fig. 4 by the symbol T (for transmit) wherever they apply. A clock generation and distribution board accepts the output of a 650-MHz oscillator and converts it into GaAs logic levels in complementary pairs of clock, clock/2, clock/4, and special pulsed clock/4 signals. All outputs, brought out on subminiature Amphenol (SMA) connectors for interconnection with the other system components, are aligned to within 50 ps. A second board, identical to the first, is used to drive equipment associated with the FTE (discussed later), although much of the clock distribution is done internally to the FTE ASIC.

Digital electronics implementation.—Figure 7 shows a typical CTE circuit board fabricated with PicoLogic IC's mounted on a prototype board developed by GigaBit Logic.[4] For the high-speed logic circuits being implemented, issues
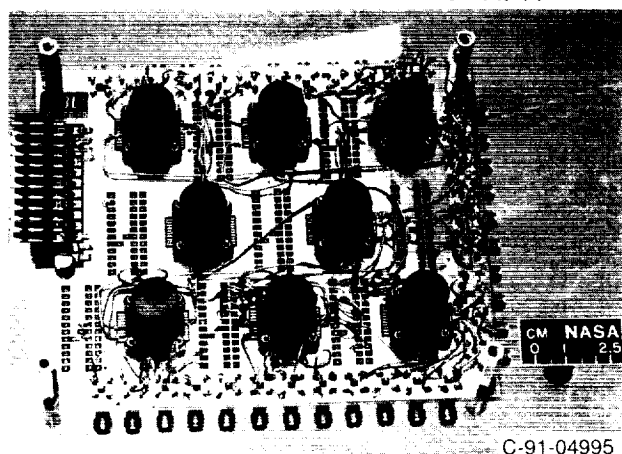
Figure 7.—Typical Hi-LITE digital prototype board.

such as propagation delay, signal interconnections and terminations, unused inputs and outputs, ac coupling, and high-frequency decoupling requirements must be carefully considered. All signal paths must be treated as transmission lines instead of simple conductors. Controlled impedance interconnections of all high-speed digital signals using semi-rigid, microcoaxial cable terminated with their characteristic impedance (typically 50 ohms) are employed to prevent signal overshoot and reflections.

Special attention must also be given to fanout. Each PicoLogic IC output is capable of driving two terminated lines while maintaining the proper voltage swing at the full rated speed. Multiple fanout buffers are generally used, although series termination and daisy-chaining are other ways to distribute signals. Unused input pins must be tied to logical high or low levels, but unused output pins may be left open to avoid wasting power in the termination resistors. Incoming signals with other than GaAs logic levels may have to be ac coupled and dc level shifted to cross the required logic threshold of -1.3 V. A substantial number of decoupling capacitors are required to isolate all power supplies and power pins from transients.

The physical layout of the circuits on the prototype boards is complicated by the high operating speeds. Typical Pico-Logic IC propagation delays of 600 ps coupled with interconnection cable delays of about 50 ps/cm are significant at 650 MHz, where the clock period is only 1538 ps. Consequently, the development and debugging process becomes iterative, where cable lengths are simulated for the desired layout and then trimmed to length on the board to achieve proper signal timing.

Receiving Electronics

High-speed, direct-detection, free-space optical communications require receiver gain control because input signal levels (analog) fluctuate but the data and clock recovery subsystems (digital) expect constant input signal levels. These fluctuations are caused by optical pointing, acquisition, and tracking errors and occur at rates of up to 1 kHz. It is the function of the analog signal conditioning (ASC) electronics to remove these signal imbalances before any data decoding can take place (Fig. 4).

Once the signal is restored to nominal levels, the receiving electronics can begin to perform its two primary operations, clock and data recovery. The slot clock recovery assembly extracts a clock operating at the slot rate of 650 MHz from the conditioned QPPM waveform. Next, the symbol clock recovery assembly further ascertains the symbol boundaries and supplies the submultiple clock rates to the receiving electronics.

The raw data recovery assembly is the first step in the conversion from the analog QPPM waveform to the high-speed binary data stream originally transmitted. A matched filter is sampled at the slot clock frequency, and its output is split and delayed by multiple slot-time increments and sent to a maximum-likelihood comparison circuit to determine which of four slots has the maximal energy. Once determined, this information is decoded into a 2-bit parallel format in the QPPM decoder. The information is then passed through the bit de-interleaver to reverse the mixing process if performed by the transmitting electronics. These signals may then be optionally converted to a single serial data stream in the channel data multiplexer or passed directly. Finally, the ambiguity resolution and sink data demultiplexer circuits convert the data's format (either single 650 Mbps or dual 325 Mbps) to that of the data sink.

Analog signal conditioner.—The ASC consists of high input signal limiting, low-pass filtering, automatic gain control (AGC), manual gain control, linear amplification, and power splitting. The ASC is designed to have a -3dB bandwidth of 700 MHz, a 35-dB dynamic range, and less than 10 dB of noise figure. When in the automatic mode, it will regulate itself to produce a constant output signal level so that the proper signal levels will be delivered to the data and clock recovery subsystems. It will also protect itself from potentially damaging high input signals.

The received signal is passed through an automatic gain control circuit that preserves the relative amplitude differences between adjacent slots while smoothing out the low-frequency (<10 kHz) amplitude fluctuations caused by mispointing. The AGC amplifies weak signals, attenuates strong signals, and lets nominal signal levels pass through without amplification or attenuation, thus producing a nearly constant peak output level while preserving the QPPM symbol structure. This result is obtained without saturating the signal, and amplification is applied only when necessary.

A block diagram of the ASC is shown in Fig. 8. The first element of the subsystem is a limiting amplifier. One of its functions is to protect the vulnerable system components (e.g., amplifiers) from very high input signals that could damage them. Another function is to provide a low noise figure for the system because the variable gain control (VGC) amplifier selected (NEC UPG106) for this design has a noise figure that is greater than the 10 dB specified by Goddard. Because the limiting amplifier has gain in its linear region, an
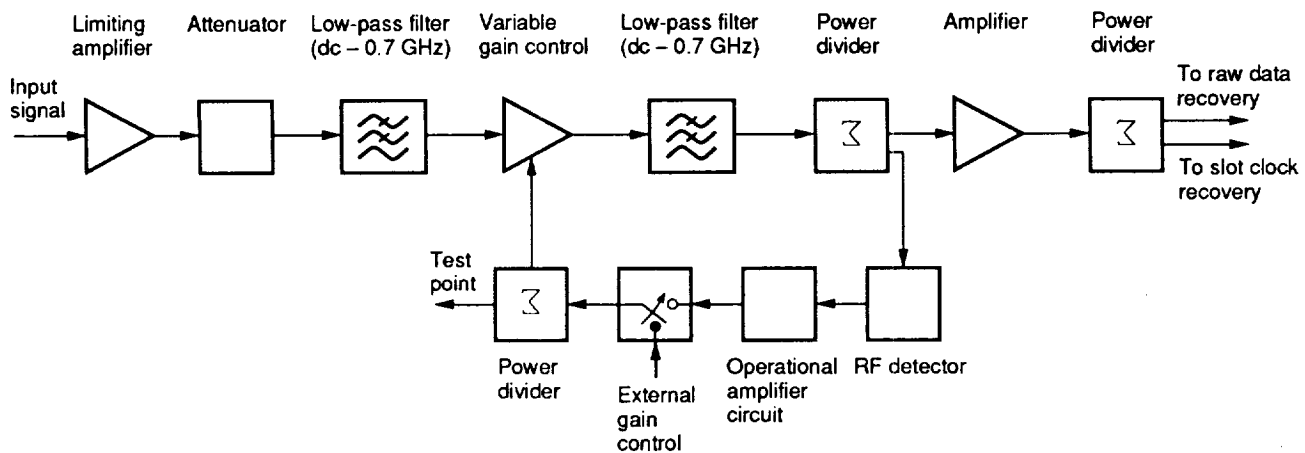
Figure 8.—Block diagram of analog signal-conditioning subsystem.

attenuator is placed at its output. It will attenuate the signal to its original received level (i.e., offset the amplification). This attenuator will also reduce the output signal power of the limiting amplifier, which might be too high for the VGC amplifier to accept. The attenuator is followed by a low-pass filter to eliminate high-frequency noise.

The filtered signal is input to a VGC amplifier. This amplifier has a voltage-controlled gain range of 35 dB and an operating frequency range of 100 kHz to 2.5 GHz. It will either increase the signal amplitude, allow it to go through unchanged, or attenuate it depending upon its received level, to provide the required dynamic range. The control can be either manual, where an external voltage can be applied to the VGC amplifier, or automatic, where a closed loop (operational amplifier) circuit provides the feedback. Another low-pass-filter follows the VGC amplifier, reducing any high-frequency noise created by the amplifier.

At the output of the filter a power divider splits the signal. One line goes into a radiofrequency detector to convert the high-frequency signal into a dc-like voltage output. An operational amplifier circuit amplifies this voltage to a level that is compatible with the VGC amplifier's control voltage requirements and low-pass filters it to 1 kHz. The other line of the power divider goes into a linear amplifier to precompensate for any downstream attenuation due to power dividing. The outputs of the second power divider are delivered to the raw data and slot clock recovery circuits.

Two identical ASC circuits will be built, one for each channel. The VGC amplifier and its control loop circuitry will be fabricated on a prototype printed circuit board. The rest of the ASC will be mounted on plates and interconnected with SMA connectors.

Slot clock recovery.—The slot clock recovery circuit extracts a 650-MHz slot clock from one of the two received QPPM waveforms provided by the ASC circuits. As long as timing skew between the two channels can be maintained within one-half of one slot time (±769 ps), only one clock recovery circuit is necessary. This circuit incorporates both analog and digital clock signal-conditioning circuits, followed by a phase-locked loop (PLL) as shown in Fig. 9.
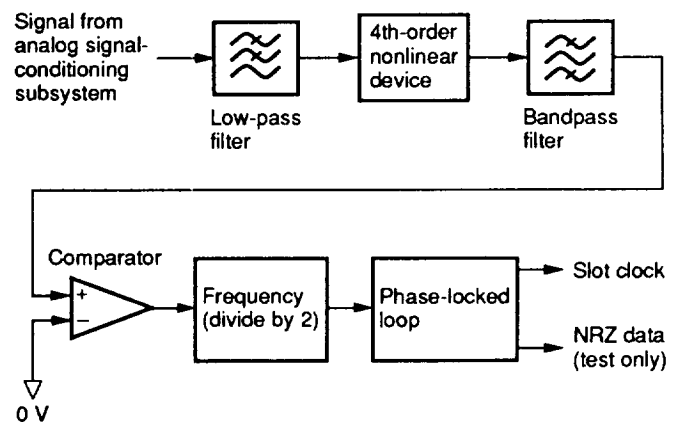

Figure 9.—Block diagram of slot clock recovery.

The signal first passes through a low-pass filter to again limit the high-frequency noise. Next, it is sent through a fourth- order nonlinear device to generate the needed harmonics at 650 MHz.[5] The desired harmonics are then isolated from the rest of the signal by a narrow-bandpass surface acoustic wave (SAW) filter. This signal is then fed into a comparator that converts the filtered analog signal to GaAs logic levels. Once in a digital format, the signal is sent through a flip-flop to halve its frequency to 325 MHz, which resembles a 650-MHz, 25%-duty-cycle nonreturn-to-zero (NRZ) waveform. The resulting signal is the optimal type for use by the commercial clock and data recovery modules designed for guided optical communications receivers.

Raw data recovery.—The purpose of the raw data recovery portion of the receiving electronics (Fig. 10) is to produce an NRZ GaAs logic level version of the received QPPM waveform. The matched filter will produce a triangular pulse shape[6] from four nominally square input pulses derived from the received QPPM waveform and delayed by four delay elements, each offset by one-quarter of a slot-time increment τ_s. The prototype QPPM filter was implemented in microstrip on RT/Duroid 6010 microwave laminate. This ceramic-polytetrafluoroethylene (PTFE) composite provides a high
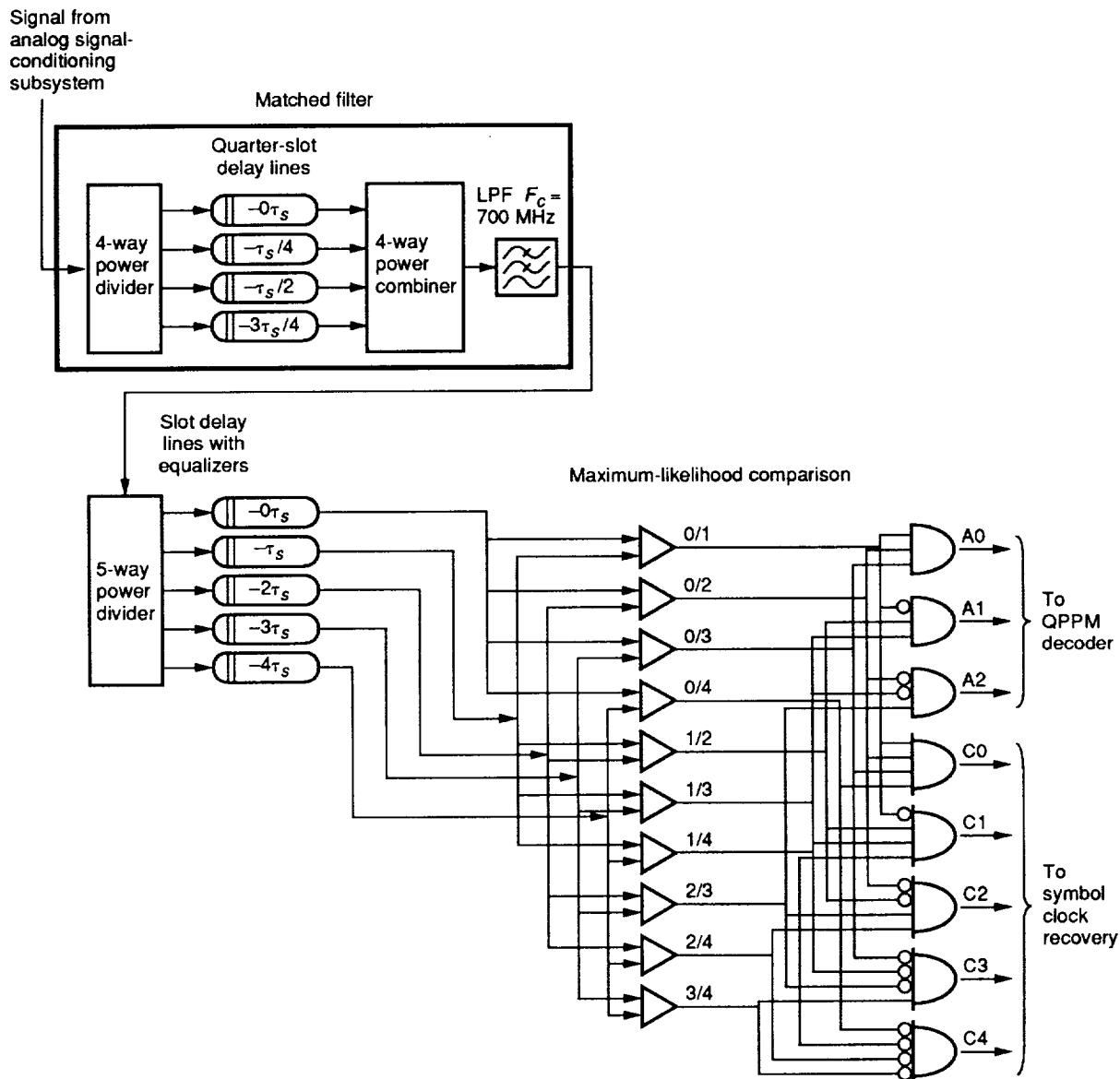
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Figure 10.—Block diagram of raw data recovery (channel A shown).

dielectric constant ($e_r = 10.2$) to minimize size while maintaining a dielectric loss tangent of less than 0.003. Total attenuation for a 50-ohm line is about 0.1 dB/in. at about 1.3 GHz for this material. As a compromise between the lithography process and the risk of generating higher order modes, a 0.025-in.-thick substrate was selected. (A thin substrate requires narrow lines, whereas a thick substrate can generate transverse surface waves.) The circuit consists of a broadband 1:4 Wilkinson power divider, four delay lines of incremental delay $nt/4$, a broadband 4:1 Wilkinson power combiner, and a 1.3-GHz low-pass filter. Total board size is about 8 in. by 25 in. In order to improve accuracy, the effect of dispersion was included in the delay line designs. The delay can be specified as

$$t = -d\phi/d\omega = -\Delta l/v_g$$

where ϕ, ω, Δl, and v_g are the phase, radian frequency, incremental length, and group velocity, respectively. The group velocity is

$$v_g^{-1} = d\beta/d\omega = e^{0.5}/c + (\omega/c)de^{0.5}/d\omega$$

where β is the propagation constant and c is the speed of light in vacuum. A closed-form expression for the frequency-dependent permittivity e was taken from Pramanick and Bhartia.[7] The group velocity at 1.3 GHz was calculated to be 1.1489×10^8 m/s. As configured, the circuit should allow reconstruction of eight sinusoidal components of the pulse given a 1.3-GHz input signal bandwidth. Figure 11 illustrates the performance for an arbitrary QPPM symbol sequence with a pulse width of 1.538 ns (1/650 MHz). In order to extract the raw data from the received signal, limited in bandwidth by the APD and preamplifier to 700 MHz, a matched filter/equalizer
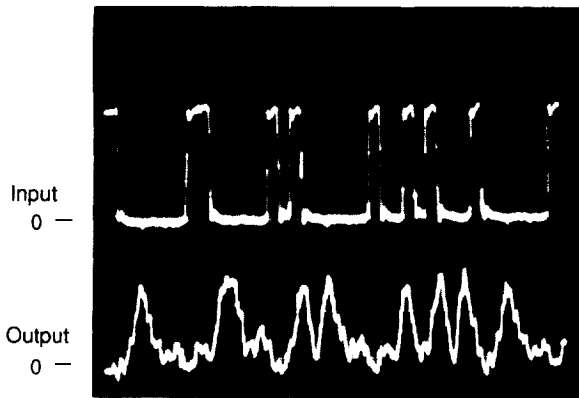
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Figure 11.—Performance of matched filter on an arbitrary QPPM sequence. Data rate, 325 Mbps (single pulse width = 1/650 MHz). Vertical: 800 mV/division; horizontal: 2 divisions represent 1 QPPM symbol (6.15 ns).

that produces raised cosine output pulse shapes from noisy trapezoidal input pulses is under development for the next version.

The matched filter feeds a five-way power splitter (Fig. 10). Each of the five signals is delayed by zero to four slot times τ_s, respectively, and is amplitude equalized and four-way power split. Amplitude equalization is critical because each line will have a different insertion loss, which must be corrected for the maximum-likelihood comparison circuit that follows the splitter. The four-way maximum-likelihood data comparison circuit uses 6 of the 10 comparators to compare the energy of each QPPM timeslot with all others, so that the slot with the most energy can be declared a logical 1. The five-way comparison circuit uses all 10 comparators to facilitate symbol clock recovery.

Symbol clock recovery.—The location of the symbol boundaries is determined by using the recovered slot clock and the NRZ logic level interpretation of the raw QPPM data. The symbol clock recovered for one channel is used to establish symbol boundaries for both channel data streams. One method of discerning symbol boundaries is to detect back-to-back pulses present only when a $(30)_4$ or $(00011000)_2$ two-symbol sequence is received in the data stream. According to the definition of the QPPM symbols, a symbol boundary must occur between the two pulses. However, the $(30)_4$ pattern cannot be detected by using the four-way comparators of the maximum-liklihood circuit until symbol boundaries are established. A second phase-locked loop (PLL) could be used to create the symbol clock.

Back-to-back pulse detection derived from the raw QPPM signal (by using threshold comparison, a one-slot delay, and a 2-bit AND gate) could be used to lock the PLL frequency to the incoming data. Because a PLL is more difficult to integrate into an ASIC than is combinatorial and sequential logic, a mostly digital clock recovery technique was developed. The symbol clock recovery circuit for the CTE is a significant portion of the receiving electronics, occupying three

full prototype boards, although the concept is straightforward and well-suited to ASIC implementation. A five-way analog level comparison among adjacent slots using all 10 comparators locates a logical 1 among four logical 0's. A "definite 1" is defined as a bit that all five of the comparisons have declared to be a logical 1. When a pattern consisting of four logical 0's surrounded by definite 1's occurs, one of the four possible symbol boundary locations can be eliminated from contention.

The circuit to resolve symbol ambiguity has to search out all possible five-way combinations of the received data and locate three consecutive blocks of four logical 0's separated by individual logical 1's (e.g.,...1000010000100001...). One solution is to sample the comparator outputs, store them in a series of shift registers, and then check the shift register outputs for the desired pattern; this solution is illustrated in Fig. 12. Part of the pattern chosen to resolve symbol timing ambiguity is $(0123)_4$ or $(1000010000100001)_2$. This inner pattern contains three blocks of four logical 0's in a row, and in the space of only four QPPM symbols it can completely eliminate three erroneous symbol boundary locations from contention.
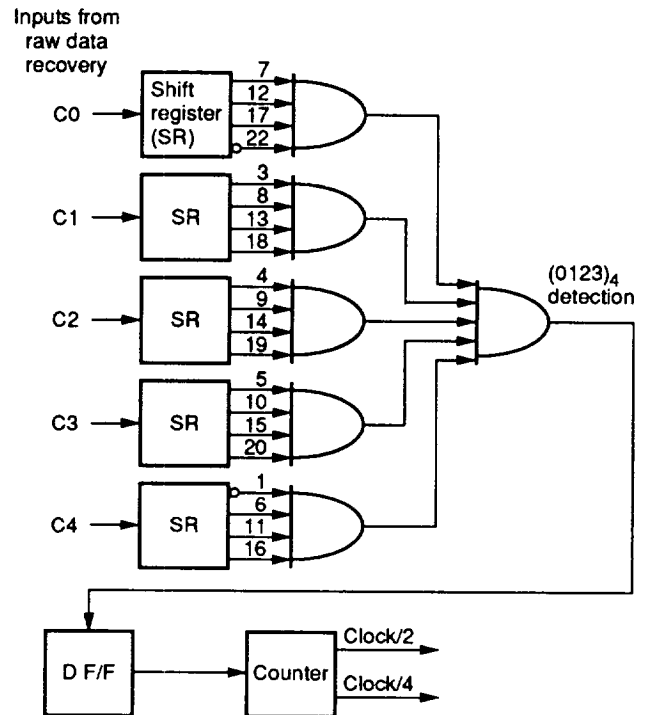

Figure 12.—Block diagram of symbol clock recovery.

The actual synchronization pattern used (i.e., $0xxxx1000010000100001xxxx0)_2$ was expanded to prevent ambiguity created by two $(0123)_4$ patterns overlapping in time by, for example, five bits $(1000010000100001)_2$. Symbol clock timing recovery is possible whenever this bit pattern occurs in the data stream. Resynchronization can be enabled at either the first occurrence or every occurrence of this pattern. Note that this circuit operates continuously with no preestablished symbol boundaries at 650 Mbps. The advantages of this method over a PLL implementation are that it reuses much of the maximum-likelihood circuitry and it can be
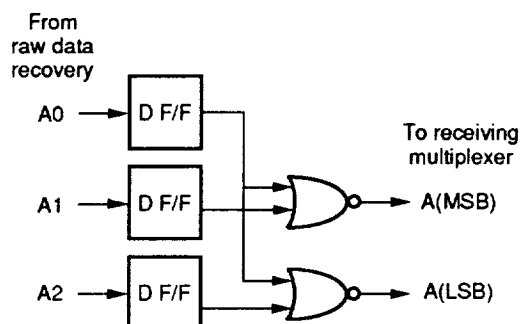
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Figure 13.—Block diagram of QPPM decoder (channel A shown).

more easily integrated into an ASIC for the flight-like version of the electronics.

QPPM symbol decoder.—Once the symbol clock has been recovered, the QPPM symbol decoder converts each channel symbol into two-bit parallel data. The 6 bits of data from the four-way comparator outputs are compressed into 3 bits of nonredundant information, latched by a symbol clock, and then decoded (see Figs. 10 and 13). The decoding is accomplished with NOR gates to form the most significant bit (MSB) and the least significant bit (LSB).

Channel data demultiplexer.—The final stages of the receiving electronics are the multiplexing circuits, illustrated in Fig. 14. Following bit de-interleaving (when enabled) the channel data demultiplexer (CDD) converts the 2-bit parallel data from each channel into two serial streams. The CDD also resolves ambiguity of bit destination in the bit interleaving mode. When the two channels are mixed, one PRBS and one non-PRBS, there is no way to ascertain which bit belongs on which channel after de-interleaving because no preambles or

acquisition patterns are sent. This ambiguity is resolved by randomly assigning the channels and checking the BER of the one assumed to be the PRBS signal. If the BER is reasonable (e.g., <<0.5), the channels are properly demultiplexed. If the BER is nearly 0.5 (assuming the rest of the system is functioning properly), the channels are switched.

Sink data demultiplexer.—The last of the CTE functions is the sink data demultiplexer (Fig. 14). If selected, a single 650-Mbps channel is reconstructed out of the two 325-Mbps channels. Otherwise, the two 325-Mbps data streams and their accompanying clocks are buffered and output from the CTE to a data sink as complementary differential pairs.

Flight-Like Terminal Electronics

The FTE will incorporate all of the electronic functions of the CTE plus an internal PRBS generator and a bit error detector. The objective of the FTE version is to integrate the CTE functions into an engineering model that closely resembles an actual spaceflight model in form, fit, and performance. The FTE hardware implementation and packaging focuses on reduced size, mass, and power consumption as compared with the CTE version. The FTE hardware is being designed with the potential for future space qualification with only minor modifications.

The FTE has been partitioned for design and fabrication purposes into a digital electronics assembly and three analog assemblies: analog signal conditioning, clock recovery, and data recovery. Although a single digital ASIC will contain all the transmitting and receiving digital circuits for both channels, each of the analog assemblies will be implemented in duplicate, one for each channel.
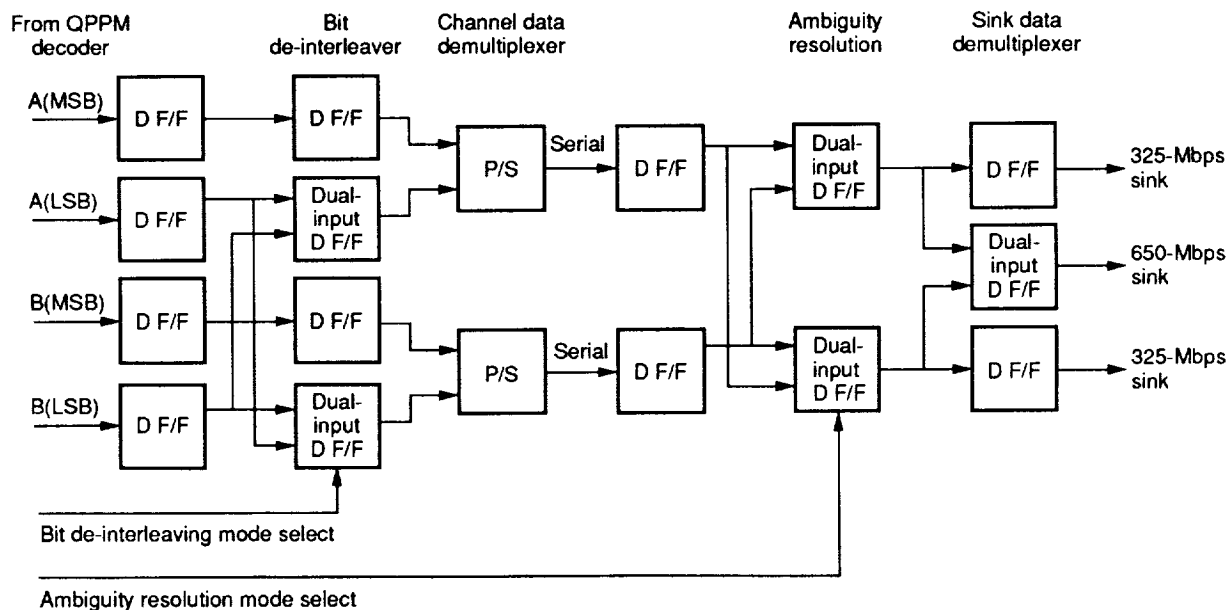

Figure 14.—Block diagram of CTE receiving multiplexer/demultiplexer.

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FTE Digital Electronics

The FTE transmitting electronics performs the same functions as its CTE counterpart. In addition, the FTE will include an internal PRBS data generator operating at 325 or 650 Mbps for use in self-contained evaluation of link performance and to aid in system pointing, acquisition, and tracking.

The internal data generator creates the 2^{23}-1-bit PRBS specified by the International Telephone and Telegraph Consultative Committee (CCITT) O.151 recommendation. The PRBS generator, clocked by the external crystal oscillator, will operate at the oscillator center frequency and one-half that rate. The binary PRBS data will be available as output from the chip for use in a variety of applications.

In addition to the standard modes of operation performed by the CTE (processing two external data sources at 325 Mbps or a single data source at 650 Mbps), the FTE will use the internal PRBS generator for operation in both modes with no external data sources. This internal data generation capability along with the associated bit error detection circuit allows the data multiplexers and bit interleavers to be tested. In a self-test mode the digital electronics should not produce any bit errors, so that the noise-free performance of the analog electronics can be determined independently.

The FTE receiving digital functions augment those of the CTE described earlier (slot and symbol clock recovery, raw QPPM data recovery, QPPM symbol decoder, channel data demultiplexer, bit de-interleaver, and sink data demultiplexer) with the addition of bit error detection capability.

The bit error detection and counter (BEDC) circuit on the receiving side is the complement of the PRBS generator on the transmitting side of the digital electronics. The BEDC circuit will selectively detect and count bit errors on decoded QPPM data from output of the sink data demultiplexer, either channel's 325-Mbps data stream, or the single reassembled 650-Mbps data stream. The BEDC latches any 23-bit segment of the recovered data sequence and creates an appropriate seed word to regenerate the error-free data sequence from the next bit forward. Note that only an error-free 23-bit segment will allow an error-free data sequence to be regenerated. The error-free sequence will then be compared, bit by bit, with the received data stream. A 23-bit segment with errors will create a data sequence that quickly exceeds an internal threshold, triggering the capture of another 23-bit segment.

The BEDC output will be presented in two forms for external bit error rate computation. First, the actual compared data will be output as a continuous serial data stream. Bit locations in error will contain a logic high. Second, a 16-bit binary count of the number of errors will be available to be latched by an external strobe. Up to 65 536 bit errors can be counted between external strobes. Once the error count is latched, the counter is reset and begins counting for the next time period.

The 16-bit error count may be used to compute bit error rates in the following manner: The BER is equal to the number of bits received in error divided by the total number of bits received during that period. The number of bits in error is given by the 16-bit error count. The total number of bits in the period is equal to the number of bits received between the consecutive rising edges of the external strobe. Therefore, if for example, a 1-kHz clock signal is used as the external strobe, the total number of bits received is given by

Total number of bits received = 325 Mbps x 1 s/kcycle
= 325 kbits/cycle

A strobe frequency that is a decimal submultiple of the data frequency of 325 Mbps is used to compute BER directly from the error count data. For example, Table II shows the total number of bits received when strobing at submultiples of the 325-Mbps data frequency.

Therefore, if the number of bits in error from the BEDC

TABLE II.—RELATION OF STROBE FREQUENCY TO BITS RECEIVED

Strobe frequency, kHz	Number of bits received
325	1000
32.5	10 000
3.25	100 000
0.325	1 000 000

counter is n, at a strobe frequency of 325 kHz

$$BER = \frac{\text{Number of bits in error}}{\text{Total number of bits received}} = \frac{n}{1000} = n \times 10^{-3}$$

and at a strobe frequency of 32.5 kHz

$$BER = \frac{\text{Number of bits in error}}{\text{Total number of bits received}} = \frac{n}{10\,000} = n \times 10^{-4}$$

It can be seen that the mantissa of the BER is simply the error count output and that the exponent is determined by the strobe frequency. Such a BER computation method will be used in the Hi-LITE subsystem to facilitate BER measurement at intervals as short as 1 ms.

Implementation Approach

The custom digital gate array will be fabricated in emitter-coupled logic (ECL) from designs developed at Lewis on Daisy-DAZIX workstations. The gate array will be mounted on an in-house-designed printed circuit board along with a crystal oscillator. The ASIC gate array will be designed to operate from dc to the highest operational frequency specified (650 MHz for the Hi-LITE subsystem).

FTE Analog Electronics

Candidate implementation techniques for the analog circuits include printed circuit boards with surface-mount devices, multichip modules, monolithic integrated circuits, analog

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ASIC's, microstrips, or hybrid circuits. Certain functions are best implemented with specific packaging techniques. For example, the low-pass filters (below 1 GHz) are best implemented as a miniaturized printed circuit board, but the slot-timing delays are best implemented in microstrip lines or coaxial cable. Current surface acoustic wave (SAW) technology, while significantly reducing the size of the delay line, cannot provide the delay accuracy required. For instance, the longest slot-timing delay required in the data recovery subsystem of one symbol period is approximately 18 in. in free space. In a SAW device this length is reduced by a factor of 100 000, which approaches the limit for placement of bond wires. The active components (limiting amplifier, voltage-controlled gain amplifier, active loop filter, and comparators) have a relatively low pin density and provide the greatest opportunity for miniaturization.

The receiving analog FTE circuits are being designed and simulated by Lewis. The circuits are simulated on the EEsof OmniSys version 3.0 systems simulator. OmniSys is used to simulate linear and nonlinear radiofrequency assemblies in both the frequency and time domains. The simulator can also optimize and adjust individual component parameters for peak system performance. Measured component performance data can be used directly with the simulator. Results of the simulation are used to evaluate potential designs before committing them to hardware. The flight-like analog assemblies will be implemented under contract from Lewis-provided circuit diagrams, component lists and specifications, signal power levels, dc power requirements, simulation data, breadboard schematics, breadboard test data, oscillograms, and interface requirements.

FTE Size, Mass, Power, and Performance Comparison

It is expected that the FTE digital electronics implemented as an ASIC gate array will consume approximately 3 W, and reside with the crystal oscillator on a printed circuit board of about 5 by 6 in. In comparison, the CTE digital electronics will consume approximately 84 W and require 12 prototype boards of approximately the same dimensions as the one FTE digital electronics board. The size and mass reductions are each expected to be about a factor of 12.

Duplicate analog electronics assemblies for two channels are expected to fit within an 8 by 8 by 2 in. enclosure. Tighter design of the signal levels in the FTE version is required to reduce power consumption to a minimum. In the FTE version, overamplification of the signals between components is minimized, thus limiting the use of attenuation and reducing power consumption.

Special Test Equipment

In order to aid the development and testing of the various elements of the Hi-LITE subsystem, special test equipment

(STE) will be designed and built at Lewis. Figure 4 indicates where the STE simulates the effect of the optical link during testing. The primary functions of the STE are to generate additional test signals and to simulate some of the optical link degradations that the CTE and FTE receiving electronics will have to accommodate.

Two forms of STE are used in testing the Hi-LITE subsystem. The digital STE consists of a test data source, channel timing jitter simulation, and interchannel timing skew simulation. The analog STE includes the simulation of noise and amplitude fluctuations induced by optical telescope pointing error and vibration. Also included under STE is the simulation of Doppler frequency shift.

Test Data Source

The purpose of the test data source (TDS) is to provide a short, repetitive pattern for initial debugging and development of some of the Hi-LITE subsystems. The TDS is used primarily in conjunction with a high-bandwidth sampling oscilloscope to assess signal quality, timing alignment, and logic circuit operation. The TDS is another source of data that, along with the commercial BER test set and video sources, is used for testing in the multiplexed data mode. The Hi-LITE assemblies that may be exercised by the TDS are designated in Fig. 4 with the diamond shape around a pulse pattern.

The output of the TDS is a switch-configurable, repetitive 32-bit pattern, clock, and pattern synchronization pulse. All outputs are GaAs logic level complementary pairs.

Timing Jitter

Timing jitter is a signal degradation inherent in the recovery of a clock from a signal in the presence of noise that is due primarily to the avalanche photodetection and matched filtering processes. Two channel timing jitter simulators will simulate the effects of jitter on the CTE and the FTE.

A separate simulator board is required to operate on each of the two QPPM data channels. Each may be independently configured for jitter intensity as desired for a given test.

The simulator intentionally adds timing jitter to the signal output from the QPPM symbol encoder. The jitter-degraded signals may be fed directly into the clock and data recovery circuits (in an all-digital, back-to-back test configuration), or through the analog STE into the analog signal-conditioning circuitry to test both analog and digital receiver performance.

Figure 15 shows a block diagram of the jitter simulator circuit. Inputs are the 325-Mbps QPPM-encoded channel data from the QPPM symbol encoder, a 650-MHz clock, and an initialization pulse from the EGSC. Outputs are the data (with imposed timing jitter) and a stable clock. These are fed either directly to the clock and data recovery circuits on the receiving side of the CTE and FTE or through the analog signal-conditioning circuitry.
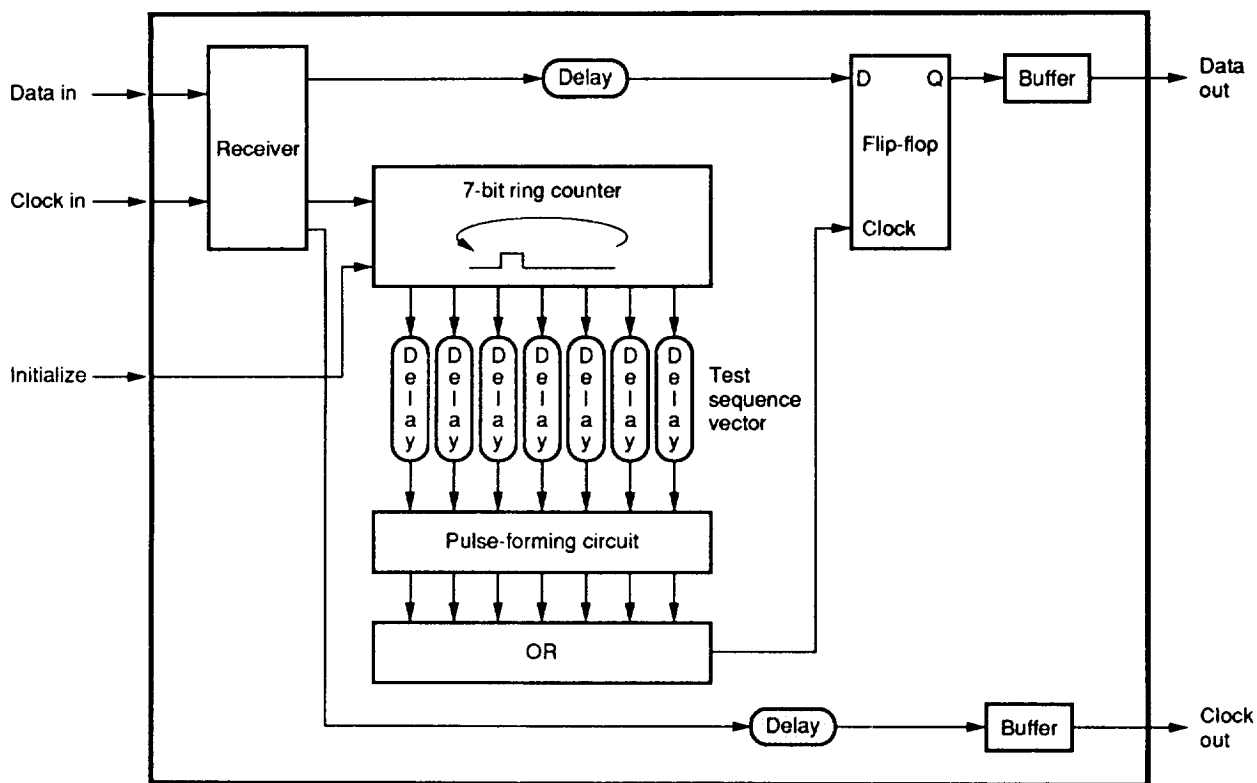
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Figure 15.—Block diagram of special test equipment for channel timing jitter simulator.

Jitter is created by the cyclical application of a seven-element timing sequence vector to the QPPM data stream's slot-time boundaries. Each element of the vector is one of three states: advanced (A), delayed (D), or unchanged (U), so that the resulting slot-time boundaries will cycle in a sequence that repeats every seven slot times. Because each QPPM symbol occupies four slot times, a pseudorandom jitter pattern is imposed upon the data stream. Any time a level transition in the QPPM data stream coincides with an advanced or delayed slot-time boundary, jitter results.

The ensuing QPPM data stream with jitter consists of five basic pulse types, as shown in Fig. 16. A computer model of the channel timing jitter simulator has been generated to calculate the relative distribution of these five pulse types for a given vector applied to a pseudorandom QPPM data stream. This quantitative prediction of the jitter severity may be used as an aid in selecting the vectors for a particular test.

The timing sequence vector is hardware programmable by means of plugging in seven appropriate delay modules to produce the desired combination of advanced, delayed, or unchanged slot-time boundaries. The seven outputs of a ring counter (implemented with a shift register) are fed through the delay modules and then logically OR'd to drive the clock input of a flip-flop with the resulting irregular timing pattern that repeats every seven slot clock cycles. The data stream passing through the flip-flop is thus jittered and finally output through a buffer.

In principle, virtually any amount of jitter may be imposed in this manner because the changes in slot boundary timing

A advanced slot-time boundary
D delayed slot-time boundary
U unchanged

(a) Normal.

(b) Compressed.

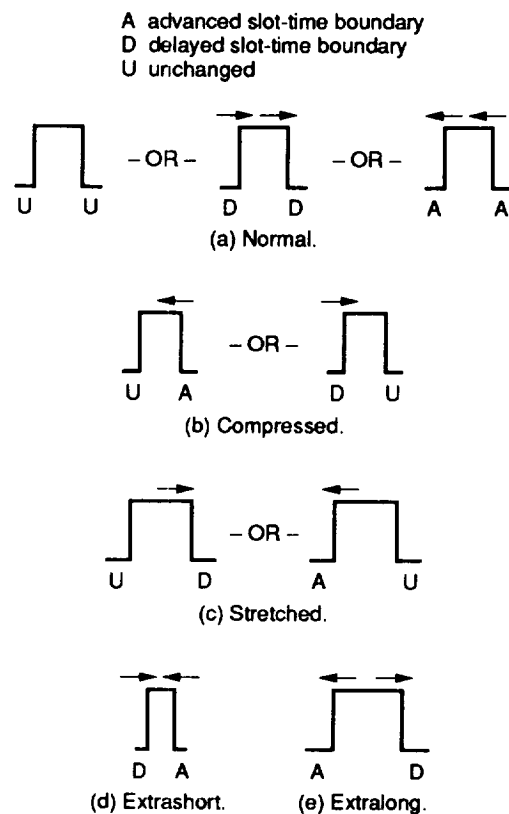(c) Stretched.

(d) Extrashort.   (e) Extralong.

Figure 16.—QPPM pulse distortion caused by special test equipment for channel timing jitter simulator.

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are directly related to the differences in the selected delay modules' time delays. A realistic maximum amount of applied jitter would be on the order of 100 ps, which is about 6.5% of the slot clock period.

Channel Timing Skew

The CTE and FTE depend on phase coherency between both QPPM data channels when the two are to be decoded and multiplexed together. Recall that the slot clock recovered from only one of the two channels is used to multiplex the two data streams back together. Therefore timing between the channels must be maintained within one-half of one slot clock period. Timing skew between the channels due to electronic and optical path differences may be simulated simply by patching different cable lengths (at nominally 50 ps/cm) while in the various test configurations. Testing with skews up to one-half of the slot clock period (769 ps), which should be significantly greater than what will be encountered in an actual link, is planned.

Noise Insertion and Amplitude Fluctuation

Inherent in a direct-detection optical link is noise that is due mainly to the statistical nature of the avalanche photodetection process. The signal is degraded by shot noise created internal to the photodetector from the signal, the background radiation, and the detector dark current, and by thermal noise from the electronic amplifier immediately following the detector, according to a Lewis internal report by R.L. Spence. In the absence of a laser transmitter and optical receiver that would provide the actual signal degradation, an appropriately modeled additive white Gaussian noise (AWGN) source is used to simulate the noise effects. In addition, amplitude fluctuation, simulating the effect of optical telescope pointing and tracking errors, can be imposed on the QPPM data signal.

These two functions are combined to form the analog special test equipment (ASTE).

Figure 17 shows a block diagram of the ASTE. Two such circuits are used to test both QPPM data channels simultaneously. The components are mounted on plates and interconnected with coaxial cable and SMA connectors. Amplitude fluctuation is achieved by means of a P-type intrinsic N-type (PIN) diode variable attenuator under control of the EGSC. To test the AGC circuits in the CTE and FTE fully, the ASTE can apply a dynamic range of at least 40 dB at a frequency of up to 1 kHz to the signal. Power meters, controlled and monitored by the EGSC, will provide signal and noise power ratio data to be correlated ultimately with the BER.

Doppler Frequency Shift

Another link effect that could be considered a signal degradation is the Doppler frequency shift due to relative motion between the transmitter and the receiver. For a link between geostationary-orbiting(GEO) and low-Earth-orbiting (LEO) satellites the resulting relative maximum velocity would be about 4.8 miles/s, impressing a Doppler shift of ± 16.8 kHz on the nominal received frequency of 650 MHz. The subsystems most sensitive to Doppler shift are the clock recovery and QPPM data recovery circuits.

In order to simulate a Doppler shift, voltage-controlled crystal oscillators (VCXO's), driven by the EGSC, are used to generate the system clocks through the clock generation and distribution boards. VCXO's with a center frequency of 650 MHz that meet the stabilities specified by Goddard (1×10^{-10} over a 10-s averaging period, for example) are commercially available, but are limited to a electrical tuning range of approximately ± 15 kHz, just short of the calculated LEO-to-GEO Doppler shift expected. In order to gain confidence in the receiving electronics' ability to tolerate Doppler shift, a VCXO with at least twice this tuning range
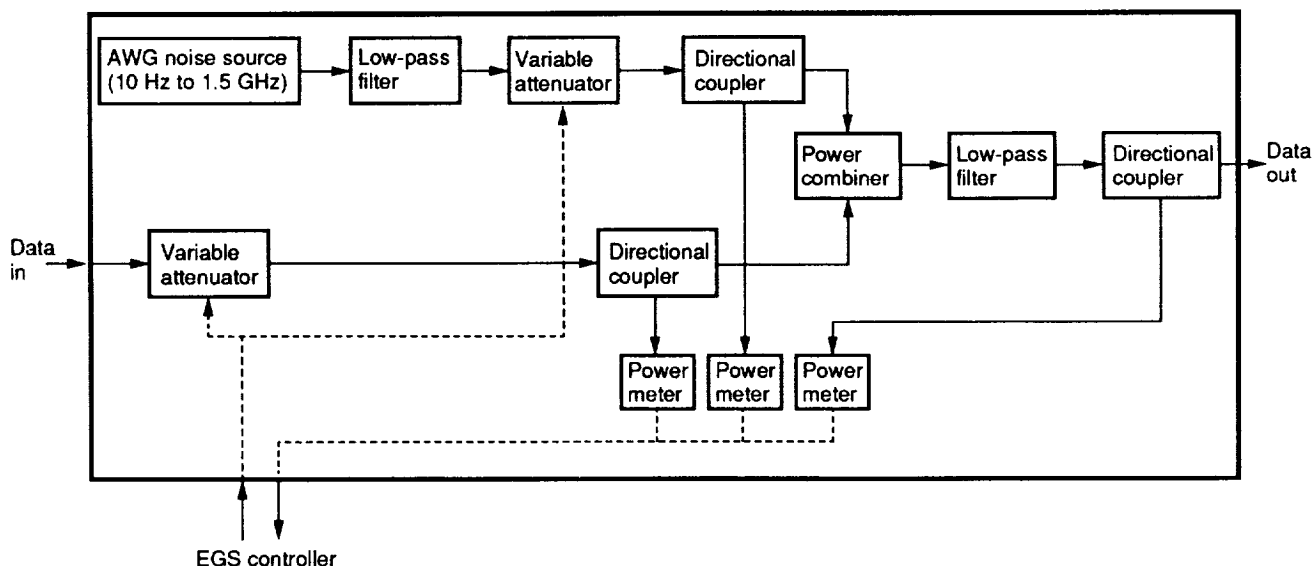

Figure 17.—Analog special test equipment.

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is employed. As a result, a less stable VCXO with a relatively high tuning range is used during the development phase for testing and debugging, to be replaced by fixed-frequency, highly stable oscillators for actual operation in the FSDD testbed.

Ground Support Equipment

Support equipment on the ground will demonstrate a complete communications system by furnishing data sources, data sinks, and computer control for spaceborne communications electronics. Generally commercial equipment, the GSE supplies pseudorandom data for BER testing, video data, and an EGSC in the form of a turnkey computer.

Bit-Error-Rate Testing

BER is the "bottom line" test parameter in characterizing the FSDD system performance. While the digital portion of the communications subsystem is expected to run error free in a back-to-back configuration (without the optical link and analog circuits), the overall FSDD is specified to operate at less than 10^{-6} BER.

Various parameters throughout the link will be correlated with BER and used to optimize the performance of the individual assemblies. Examples are the gain setting of the avalanche photodiode and the optical system's telescope alignment (pointing and tracking errors), which are instrumental in determining the minimum photon-per-bit ratio required for the APD.[8]

A PRBS of 2^{23}-1 bits in length and conforming to the CCITT O.151 standard will be used to measure BER. A commercial test set is the main source and sink for the PRBS data. As described earlier, the FTE will also be capable of generating and checking a 2^{23}-1-bit PRBS. Some of Goddard's test requirements call for BER measurements at millisecond intervals, which will be feasible with the FTE described earlier; the commercial test set is limited to a 1-s measurement rate. The bit error count provided by the FTE is readily converted to a BER by the EGSC.

For video and other real data sources, interleaving their bit streams with PRBS data provides an indirect BER measurement capability, avoiding the difficult task of actually error-checking the real data. With this method (also described earlier), a quantitative as well as a qualitative (observing the received video image on a monitor) assessment of video data transmission is achieved.

Video Sources and Sinks

Component video was chosen as the source video format to provide high-resolution images and to utilize the full FSDD channel data rate of 325 Mbps. Alternative formats such as high-definition television (HDTV) and National Television System Committee (NTSC) composite video were considered and discarded because of the increased hardware complexity, the high cost of the video equipment, or both. NTSC composite video provides lower resolution images than component video and would require significant data padding to fill the FSDD 325-Mbps channel. HDTV video equipment is currently prohibitively expensive and would require additional costly video data compression equipment to reduce the digitized video data rate to 325 Mbps.

The component video signal consists of a luminance signal, Y, and two color difference signals, R-Y and B-Y. Digital encoding of the Y, R-Y, B-Y component video consists of sampling each component at a frequency of 13.5417 MHz using 8-bit resolution. This sampling rate is slightly higher than the International Radio Consultative Committee (CCIR) recommendation 601-1 sampling rate of 13.5 MHz. The resulting composite digital rate is therefore 325 Mbps (13.5417 MHz x 8 bits x 3).

It is important for the sampling clock of the analog-to-digitial (A/D) converter to be phase locked to the video signals to avoid moiré patterns (distortion and wavy lines, generally parallel to the scanning lines) in the reconstructed image. Typically the sample clock is derived from the video horizontal synchronization frequency, but this would mean the undesirable slaving of the terminal electronics clock to the video sources. Instead, the external reference circuitry of the video source equipment is driven by a video synchronization signal derived from the terminal electronics clock. The sampling clock is also derived from the terminal electronics clock, and thus the video sources are synchronous with the sampling clock.

After digitally encoding the component video signal into 24-bit samples, a parallel-to-serial (P/S) conversion creates the 325-Mbps data stream for the source data multiplexer. On the receiving side a serial-to-parallel (S/P) conversion obtains the original 24-bit samples, from which the component video signals are reconstructed with a triple 8-bit digital-to-analog (D/A) converter. In order to resolve sample boundary ambiguity in receiving the 325-Mbps serial data stream and converting to the correct 24-bit parallel samples, a video synchronization detection circuit is used on the reconstructed video signal as an indicator of correct S/P word alignment. When no synchyronization is detected on the reconstructed signal, the 24-bit word alignment of the S/P converter is shifted one bit at a time with the feedback from the synchronization detection circuit until correct alignment is obtained.

Audio data are also encoded with the video signals. During each horizontal synchronization pulse of the video signal, a 24-bit audio sample is multiplexed into the serial data stream in place of a video sample. On the receiving side the audio and video are demultiplexed and the missing video synchronization sample is restored. This will allow audio data to be sent along with the video data at 377.6 kbps (15.734 kHz x 24 bits).

Two video data sources and two video data sinks are required to fully support the duplex FSDD communications system (Fig. 18). A camera and a video tape recorder/player

(VTR) were chosen for the video sources. The camera enables live video signals to be transmitted through the FSDD communications system; the VTR can provide a more interesting, repetitive source of video for transmitting video test patterns and for testing the effect of channel degradations on certain types of video images. The video sinks consist of two component video monitors. The VTR can also double as a video sink so that the channel effects of images can be recorded and played back for later analysis (Fig. 19).

Plans include the purchase of a hard-copy unit for documentation and presentation of the results of the video experiments. The hard-copy unit will be required to freeze and store a frame of a live component video signal and produce high-resolution color slides, prints, and transparencies of the frozen image. The outputs of the hard-copy unit will enable comparisons of transmitted and received video images, as well as comparisons of received video images subjected to a variety of channel conditions.

Electronics and Ground Support Controller

In addition to the data sources and sinks the ground support equipment includes the EGSC, enabling completely automated testing. The EGSC's main function is to provide central monitoring and control of the Hi-LITE subsystem along with data acquisition, analysis, and storage.

A 386SX personal computer is the heart of the EGSC. Commercial interface boards in a personal computer (PC) bus extender chassis allow the 386SX to communicate with the electronics and ground support equipment by means of logic level lines, analog lines, and an IEEE–488 general-purpose interface bus (GPIB) bus (Fig. 20). Software written in the C language provides a mouse-driven graphical user interface for controlling, monitoring, and acquiring data through the interface boards. Software is flexible so that new test sequences are easily generated. Goddard plans a similar PC-based system for control of all of the FSDD subsystems, which should facilitate the integration of both the Hi-LITE hardware and software.

Figure 19.—Hi-LITE video tape recorder/player and monitor.

Packaging

The packaging design of the Hi-LITE subsystem has two goals. The first is to create a chassis arrangement that facilitates operations and maintenance of the subsystem. The second is to provide an environment for the electronics equipment that will allow circuit components to achieve their designed-for lifetimes and required reliability levels. Figure 21 is a view of the subsystem rack layout. Note that in meeting the first goal, the video equipment has been grouped into one rack, the communications subsystem's electronics into another, and the EGSC computer and its associated test equipment into a third rack. The rack housing the communication electronics is a special shielded rack that meets Federal
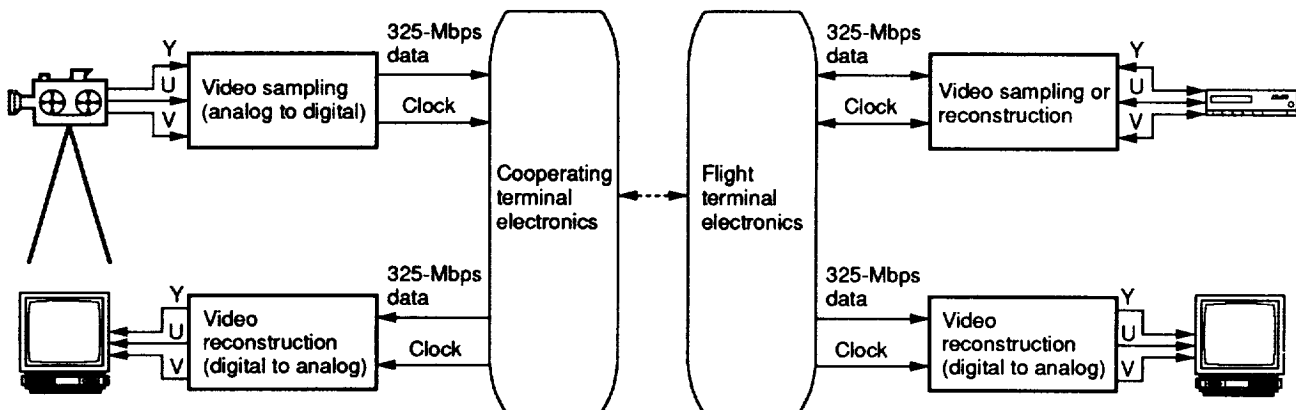

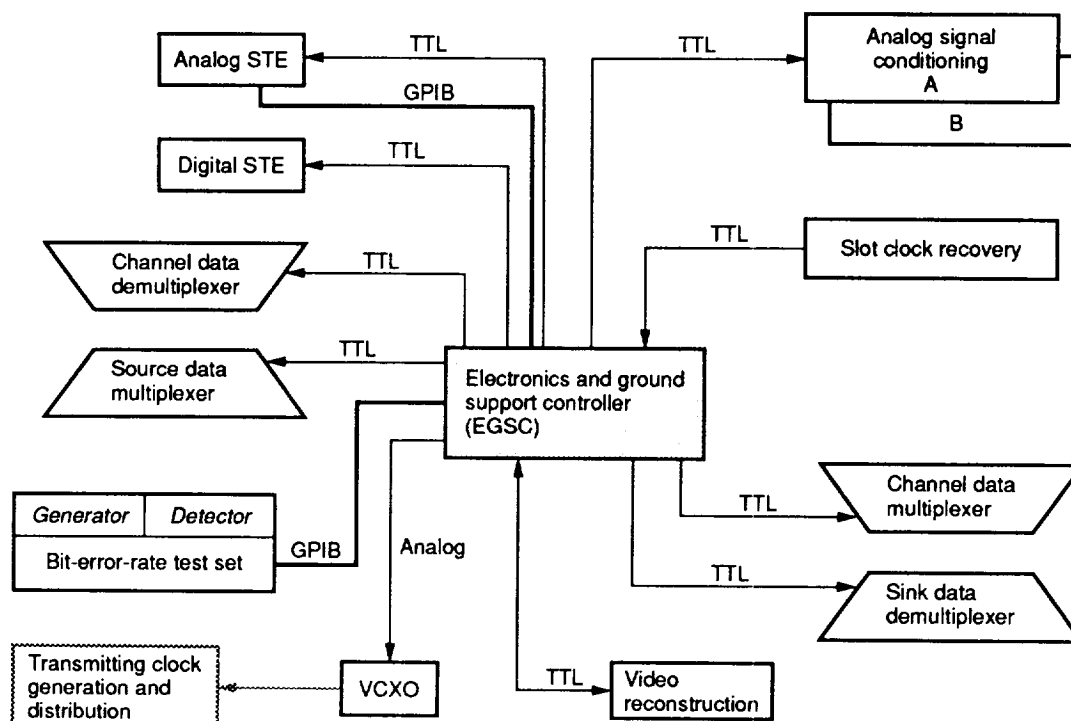Figure 18.—Hi-LITE video sources and sinks.

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Figure 20

Analog STE

TTL

GPIB

Analog signal conditioning
A
B

TTL

Digital STE

TTL

Slot clock recovery

TTL

Channel data demultiplexer

TTL

Source data multiplexer

TTL

Electronics and ground support controller (EGSC)

Channel data multiplexer

TTL

Generator	Detector
Bit-error-rate test set	

GPIB

Analog

Sink data demultiplexer

TTL

Transmitting clock generation and distribution

VCXO

TTL

Video reconstruction

Figure 20.—Electronics and ground support controller.

Figure 21

Video rack

| Fan |
| Monitor |
| Monitor |
| Video hard copier |
| Format converter |
| Camera controller |
| Video tape recorder |
| Digital video (A/D and D/A) |
| Blank |

Electronics rack

| CTE— transmitting electronics |
| CTE— receiving analog electronics |
| CTE— receiving digital electronics |
| FTE |
| Special test equipment |
| Blank |
| Fan |

Ground support equipment rack

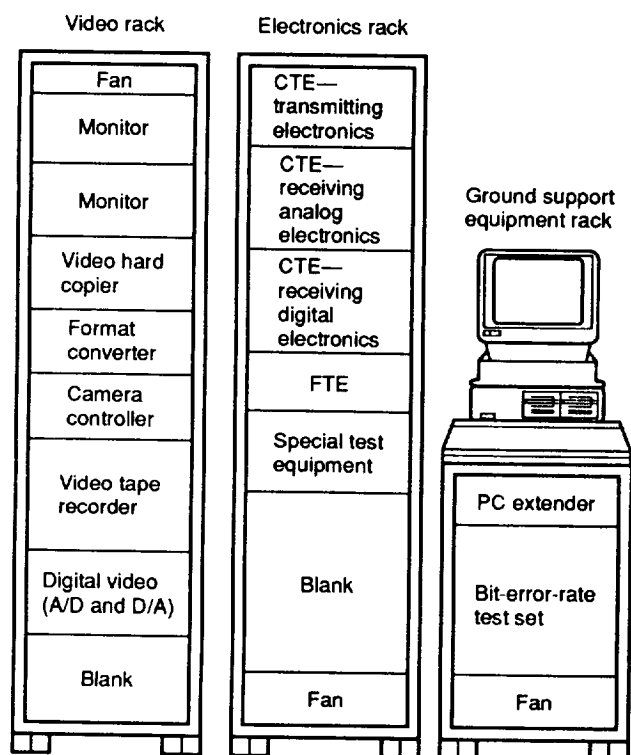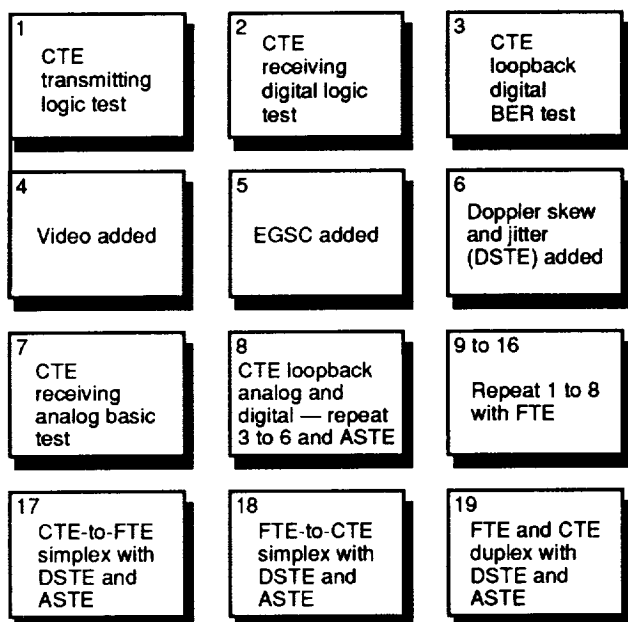| PC extender |
| Bit-error-rate test set |
| Fan |

Figure 21.—Hi-LITE rack layout.

Communications Commission (FCC) commercial standards for electromagnetic interference/radiofrequency (EMI/RF) shielding.
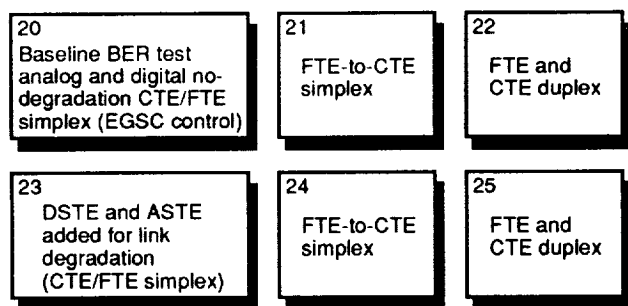
Meeting the second goal requires that secure mounting for boards and cables be achieved along with adequate cooling. The racks each contain a built-in airflow system consisting of fans and vents that provide an overall airflow throughout the racks. Small muffin fans are applied at specific locations, as required, for spot cooling of boards or components.
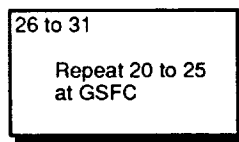
Subsystem Integration and Testing

Figure 22 shows the planned sequence for the integration and testing of the Hi-LITE subsystem. The first major part, integration, encompasses debugging and modification activity as the subsystems are combined, gradually increasing in overall system complexity. The next part, preacceptance testing at Lewis, has the goal of producing documentation that characterizes the performance of the integrated Hi-LITE subsystem by using the STE to simulate link degradations. As in integration the system under test is gradually increased in complexity. The last part of the testing, acceptance testing at Goddard, repeats the preacceptance testing after the Hi-LITE subsystem has been delivered to Goddard in order to verify its performance prior to integration into the FSDD testbed.

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1 CTE transmitting logic test	2 CTE receiving digital logic test	3 CTE loopback digital BER test
4 Video added	5 EGSC added	6 Doppler skew and jitter (DSTE) added
7 CTE receiving analog basic test	8 CTE loopback analog and digital — repeat 3 to 6 and ASTE	9 to 16 Repeat 1 to 8 with FTE
17 CTE-to-FTE simplex with DSTE and ASTE	18 FTE-to-CTE simplex with DSTE and ASTE	19 FTE and CTE duplex with DSTE and ASTE

(a) Integration (debug and modify).

20 Baseline BER test analog and digital no-degradation CTE/FTE simplex (EGSC control)	21 FTE-to-CTE simplex	22 FTE and CTE duplex
23 DSTE and ASTE added for link degradation (CTE/FTE simplex)	24 FTE-to-CTE simplex	25 FTE and CTE duplex

(b) Preacceptance testing at Lewis (characterize and document).

26 to 31 Repeat 20 to 25 at GSFC

(c) Acceptance testing at Goddard
(verify performance after delivery).

Figure 22.—Hi-LITE integration and testing sequence.

Concluding Remarks

The communications electronics and associated test and control equipment for demonstration of 650-Mbps QPPM free-space laser communications is under development at NASA Lewis. Following a successful demonstration of the communications electronics in NASA Goddard's FSDD testbed, a second copy of the flight-like version is planned for use in further laboratory experiments.

Plans also include a flight-qualified version of the communications electronics subsystem. This version would be designed for experimental use in either a low-Earth-orbiting platform or a geosynchronous-orbiting satellite, to demonstrate the capabilities and performance of optical crosslinks in free space. It will also include error encoding and correction of the information data by using block codes. An increase in total data throughput to 1.3 Gbps may be possible. Finally a technique called combinatorial PPM, under in-house development at Lewis, will be demonstrated to show increased data throughput with reduced peak-to-average power requirements for the semiconductor laser transmitter.

Appendix—Glossary

A/D	analog to digital
AGC	automatic gain control
ASC	analog signal conditioner
ASIC	application-specific integrated circuit
ASTE	analog special test equipment
AWGN	additive white Gaussian noise
BEDC	bit error detection and counter
BER	bit error rate
CDD	channel data-demultiplexer
CCIT	International Telephone and Telegraph Consultative Committee
CTE	"cooperating" terminal electronics
D/A	digital to analog
ECL	emitter-coupled logic
EGSC	electronics and ground support controller
FSDD	flight system development and demonstration
FTE	"flight-like" terminal electronics
GaAs	gallium arsenide
GEO	geostationary orbiting
GPIB	general-purpose interface bus
GSE	ground support equipment
HDTV	high-definition television
Hi-LITE	High Speed Laser Integrated Terminal Electronics Project
IC	integrated circuit
LEO	low Earth orbiting
LSB	least significant bit
Mbps	megabits per second
MSB	most significant bit
NRZ	nonreturn to zero
NTSC	National Television System Committee
PC	personal computer
PLL	phase-locked loop
PPM	pulse position modulation
PRBS	pseudorandom bit sequence
P/S	parallel to serial
QPPM	quaternary pulse position modulation
SAW	surface acoustic wave
SMA	subminiature amphenol
SNR	signal-to-noise ratio
S/P	serial to parallel
STE	special test equipment

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TTL   transistor-transistor logic
VCXO   voltage-controlled crystal oscillators
VGC   variable gain control
VTR   video tape recorder/player

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16. Abstract

The development of a high-data-rate communications electronics subsystem for future application in free-space, direct-detection laser communications is described. The dual-channel subsystem uses quaternary pulse position modulation (QPPM) and operates at a throughput of 650 megabits per second (Mbps). Transmitting functions described include source data multiplexing, channel data demultiplexing, and QPPM symbol encoding. Receiving functions include analog signal conditioning, slot and symbol clock recovery, QPPM data recovery and decoding, channel data multiplexing, and destination data demultiplexing. Implementation of a prototype version in discrete gallium arsenide (GaAs) logic, radiofrequency components, and microstrip circuitry is presented. The approach to developing an integrated package for potential spaceflight demonstration is described. Link effects simulation, full-duplex and video communications demonstration, and computer control and monitoring approaches are discussed. Packaging of the communications electronics subsystem and plans for future development conclude the paper.

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